Investigation of Forward Voltage Degradation of Silicon Carbide (SiC) pn Diode and Fabrication of High Voltage SiC pn Diode

Background

Since silicon carbide (SiC) power devices have a potential of high-voltage and low-loss compared to silicon power devices, their practical use is desired for more low-loss and miniaturized power-electronics apparatuses. On SiC pn diodes applied basic structure of semiconductor devices, degradation of a forward voltage (an on-state loss) is caused by sending a current. This issue is the most serious problem for practical use of SiC pn diodes. And high voltage devices require thick epitaxial layer, it is very important to investigate forward voltage degradation of thick layers. And we also need to investigate the degradation suppression technique. (This work is collaborated with The Kansai Electric Power Co., Inc..)

Objectives

To investigate the forward voltage degradation on SiC pn structure and fabricate high voltage SiC pn diode.

Principal Results

We fabricated SiC pn diode using SiC substrate with SiC layer made by our developed vertical hot-wall CVD reactor. And we investigated the degradation characteristics on n-type layer thickness, crystal polarities and off directions. And finally, we tried to fabricate high voltage SiC pn diode using those results (Figure 1).

1：Investigation of degradation characteristic for thick layer

It became clear quantitatively that thicker n-type layer lets to more increase degradation (Figure 2). This result shows that the degradation is serious problem to high voltage SiC pn diodes, which need thick layer.

2：Investigation of degradation suppression technique

We investigated on the degradation of crystal polarity *[1] and off direction *[2] SiC pn diode used C-face <11-20> toward off substrate is the least degradation of other substrates (Figure 3).

3：Fabrication of high voltage SiC pn diode

We succeeded in fabricating 4.55kV SiC pn diode using thick and low-doped n-type layer (~60 μm, ~6×10^{13}cm^{-3}) on <11-20> toward off C-face substrate with JTE (Junction Termination Expansion)*[3], which expands localized electric field on pn junction termination (Figure 4). This result is the highest performance in C-face SiC devices.

Future Developments

On the basis of these results, we’re going to develop low degradation, high reliability, high voltage (over 5kV) and low loss SiC pn diode.

Main Researcher: Toshiyuki Miyanagi,
Research Scientist, Material Functions and Mechanism Creation Sector, Material Science Research Laboratory

Reference

T. Miyanagi et al, 2003, “Development of process technologies for high voltage SiC pn diode fabrication
-Investigation of reduced technique for forward voltage degradation and fabrication of high voltage SiC pn diode- “, CRIEPI REPORT W03033 (in Japanese)

*1：SiC has crystal polarities called Si-face and C-face, which show different chemical characteristics. In general, Si-face is using to SiC device fabrication, because thick and low-doping layer to need high voltage devices is difficult to make on C-face substrate.

*2：SiC substrate with tilt off-cut toward specific direction is used to make same crystal structure as substrate. In general, <11-20> toward off SiC substrate is used to fabricate of SiC devices.

*3：A p-type layer like a doughnut was fabricated into n-type layer surface using ion implantation technique. By this technique, the blocking voltage become near theoretical value, because the electric field expands widely.

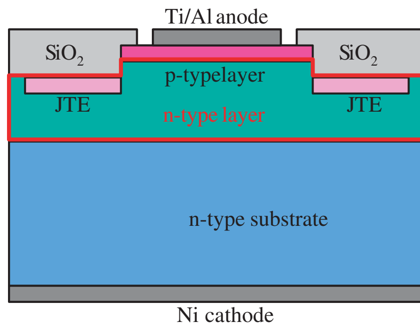


Fig.1 SiC pn diode

A n-type layer thickness defines forward voltage and blocking voltage.

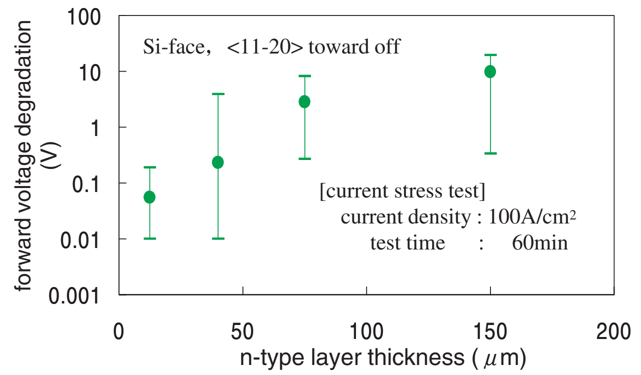
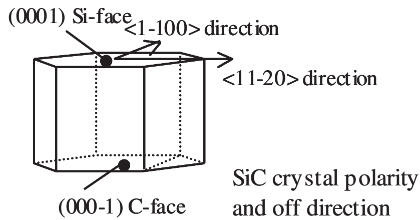


Fig.2 degradation characteristics of n-type layer thickness (size 2.6mmφ)



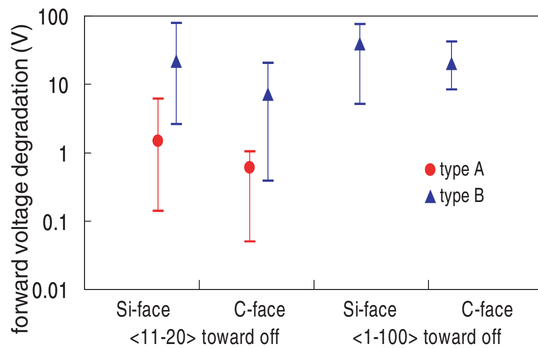


Fig.3 degradation characteristics of polarity and off directions (thickness 40 μm, size 2.6mmφ, type A and type B are made by different products.)

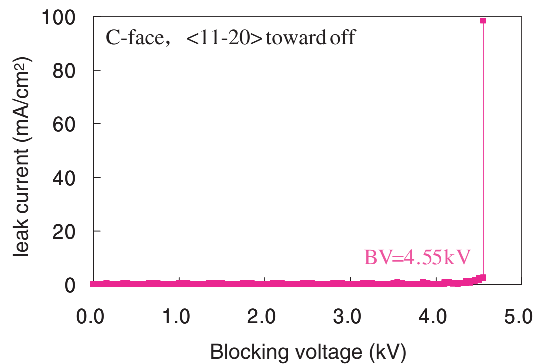


Fig.4 blocking voltage of C-face SiC pn diode (thickness 60 μm, size 0.26mmφ)