Development of SiC Epitaxial Growth Techniques with a Low Defect Density and Large Diameter and Preliminary Demonstration of Large SiC Diodes

Background

Power electronics apparatus using SiC power devices can achieve large reduction in power consumption by low-loss operation and in size of the apparatus by high-voltage blocking capability of the devices in comparison with using Si-based devices. It has been proven excellent low-loss performance in SiC devices with a small active area, however it is required to realize devices with a larger current capacity (enlargement of the device active area) and a higher blocking voltage capability for power system applications. Because of this reason, CRIEPI is developing SiC epitaxial growth techniques to reduce defects that can restrict enlargement of device area and blocking voltage of the devices and fabrication techniques of high-voltage SiC diodes [*1].

Objectives

To demonstrate the possibility of large SiC devices by fabrication of trial power diodes and to obtain thick SiC epitaxitial layers [*2] with a large diameter that can be applied in power electric apparatus for a power system and demand customer system, we develop SiC epitaxial growth techniques with a low defect density and a prototype large-area epitaxial growth reactor.

Principal Results

1. Low defect density SiC epitaxial growth and large power diode demonstration

(1) Dislocation penetration and generation in 4H-SiC epitaxal growth were investigated by Synchrotron (SPring-8) X-ray topography as shown in Fig.1. The results in Fig.2 show that a large reduction in the density of basal plane dislocations [*3] can be achieved by (i) performing (000-1)C-face epitaxial growth with a low propagation ratio of the dislocations from the substrate into the epilayer in comparison with conventional (0001)Si-face growth and (ii) growing epilayers with a low generation frequency of the dislocations at a high C/Si ratio of the source gases.

(2) The density of large in-grown defects that can act as killer defects for high-voltage blocking has been reduced down to 0.3 cm^{-2} by the optimization of the growth parameters. We succeeded in preliminary demonstration of high-current SiC diodes corresponding to 100-200 A class by obtaining a high yield of 66% for 1 cm^2 large Schottky barrier contacts with a low leakage current density through fabricating prototype SiC power diodes on the low-defect density epitaxial layer as shown in Fig.3.

2. Prototype large diameter SiC epitaxial growth reactor

Growth of 4H-SiC epitaxial layers at an average growth rate of 23 μm/h with a good thickness uniformity of 1.7 % corresponding to a production level for 4-inch diameter equivalent area has been achieved in a prototype large diameter SiC epitaxial reactor by the optimization of reactor configuration set up and growth conditions through 3D thermo-fluid computer simulation and growth experiment as shown in Fig.4.

Future Developments

We will try to put the SiC epitaxial growth technique with a low defect density and the fabrication technique of high-performance SiC diodes to practical use in the consumer and industrial applications, establish large-diameter and high-quality (low defect, high purity, thick) SiC epitaxial growth technique and develop fabrication technique of large devices.

Main Researcher: Hidekazu Tsuchida, Ph. D.,
Senior Research Scientist, Materials Functions and Mechanism Creation Sector, Materials Science Research Laboratory

References

H. Tsuchida, et al., 2005, “Growth of thick 4H-SiC(000-1) epilayers and reduction of basal plane dislocations”: Japanese Journal of Applied Physics, Vol. 44, No. 25

H. Tsuchida, et al., “Comparison of electrical characteristics of 4H-SiC(0001) and (000-1) Schottky barrier diodes”, Materials Science Forum, Vol. 527-529.

＊1：CRIEPI report (W02018) “Development of epitaxial growth techniques for high-power SiC semiconductor devices”
＊2：Crystalline SiC layer grown on a SiC substrate. Epitaxial layers are utilized as an active region of SiC devices.
＊3：Shockley-type dislocations lying on the basal plane. The dislocations cause degradation of SiC pn diodes.

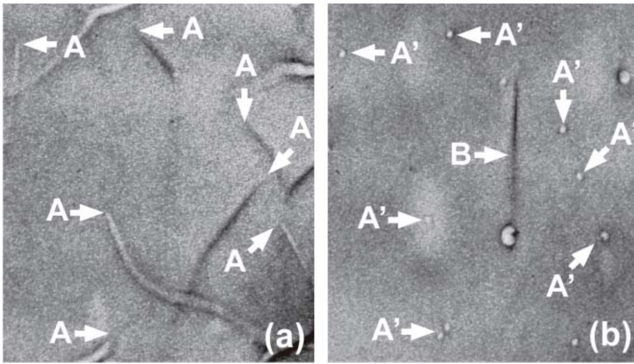

Fig.1 Synchrotron X-ray topographic images taken (a) before and (b) after 4H-SiC epitaxial growth for the same position

The images (a) and (b) indicate dislocations near the substrate surface and near epilayer surface for the same position, respectively. Propagation of the dislocations from the substrate to epilayer as A→A' and generation of a new dislocation by the epitaxial growth as marked B are confirmed.

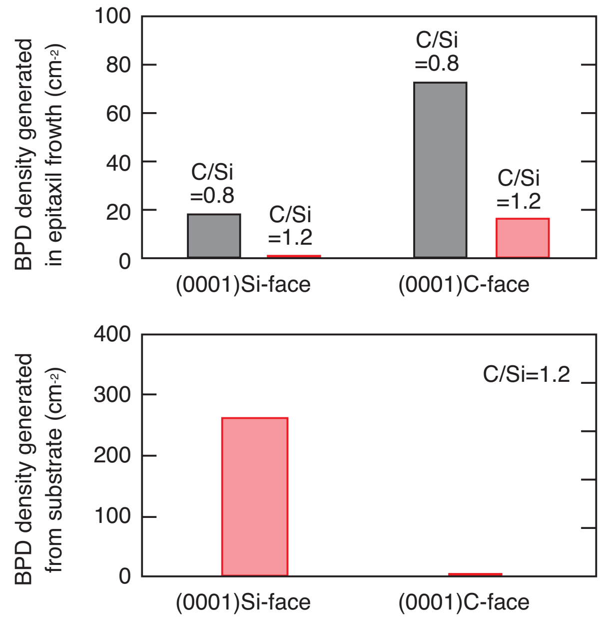

Fig.2 Propagation and generation densities ofbasal plane dislocations (BPDs) in epitaxial growth

Density of basal plane dislocations (BPDs) in 4H-SiC epilayers can be reduced by choosing (000-1)C-face as a growth face and a high C/Si ratio of the source gases.

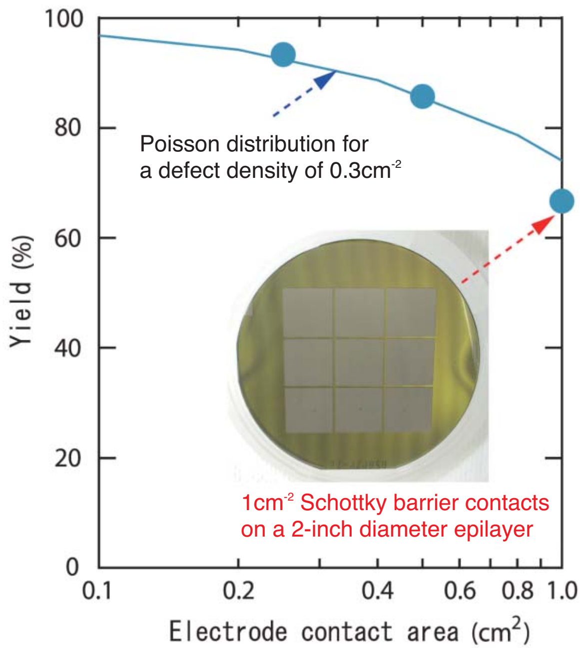

Fig.3 Yields of 0.25-1 cm^2 Schottky barrier contacts with a small leakage current density

Mo/SiC Schottky barrier contacts were deposited on 2-inch diameter epitaxial wafer and the yields of devices with a leakage current density bellow 1 x~10^{-6} A/cm^{-2} at 300 V were determined.

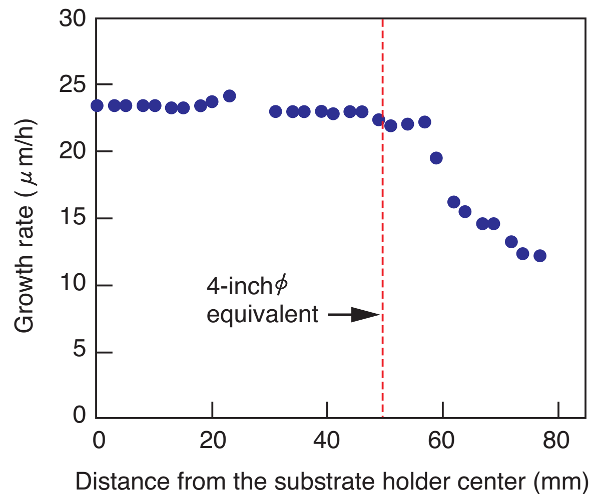

Fig.4 Growth rate uniformity of an epilayer for a prototype large diameter SiC epitaxial reactor

A good thickness uniformity with a high growth rate is obtained for 4-inch equivalent area, which can be a practical wafer diameter.