Priority Subjects with Limited Terms — **Development of a Supply/Demand Infrastructure for Next-Generation Electric Power**

Development of High-Performance SiC Power Semiconductors

Background and Objective

Development of low-loss high-voltage power conversion equipment is expected for stable power supply under mass introduction of renewable energy sources and in response to reinforcement of grid interconnection and wide-area integrated operation. Silicon carbide (SiC) power devices are potential technology to realize small-sized low-loss power conversion equipment, although practical applications of the devices are limited to low-power equipment such as air conditioners. Thick SiC crystal layers with a low defect density are essential for the development of large-capacity devices. We have obtained thick and high-purity SiC crystal layers able to accommodate very high voltage (>13 kV) devices in the use of an original SiC crystal growth reactor.

In this project, we aim to establish a practical crystal growth technology for the production of thick SiC crystal layers with a low defect density which realize high-voltage, large handling current SiC power devices.

Main results

1 Optimization of the fast SiC crystal growth process

We developed a fast SiC crystal growth (epitaxial growth) technique achieving a low defect density*1 to obtain thick, high-quality SiC crystal layers for high-power SiC devices. It was clarified that lowering the partial pressure of Si source gas (SiH_4) as well as adding HCl to the gas system prevent the formation of stacking faults in the crystal growth process even at a high growth rate exceeding a few tens of microns per hour (Fig. 1). At the same time, reductions of dislocations and point defects are achieved simultaneously by adjusting the crystallographic angles of the substrates. Based on the improvements, the densities of stacking faults and dislocations are reduced to a level which can realize large devices with ~1 cm^2 area (equivalent to >100 A class), and high-quality SiC epilayers are attained with a point defect density low enough to obtain long carrier lifetimes*2 for very high voltage devices with a application of “Carbon Interstitial Diffusion Process”*3 (CRIEPI’s original process).

2 Clarification and control of dislocation behavior for improvement in quality of SiC crystal layers

We clarified dislocation behavior and development of defect imaging techniques, aiming to prevent the degradation of electrical performance of SiC devices by controlling dislocations in SiC crystals. It was clarified that increasing the annealing temperature or performing ion implantation followed by the second epitaxial growth before Ar annealing in “High-Temperature Dislocation Conversion Process” *4 (CRIEPI’s original process) achieves a significant reduction in the BPD density of SiC crystal layers by enhancement of conversion ratios of basal plane dislocations (BPDs) to threading edge dislocations (TEDs) (Fig. 2). We also succeeded in discriminating the Burgers vector*5 of TEDs using plan-view photoluminescence (PL) imaging and direct observation of line directions of TEDs and threading screw dislocations (TSDs) by cross-sectional PL imaging (Figs. 3 and 4). These defect imaging techniques can accelerate further improvements in quality of SiC crystal layers for the development of high-performance SiC devices through more precise control of TED and TSD propagation behavior.

*1 In this study, 8H-type stacking faults, BPDs and point defects ($Z_{1/2}$ center), which degrade the electrical performance of SiC devices, are reduced to 0.1 cm^{-2}, 0.09 cm^{-2} and $1x10^{12}$ cm^{-3}, respectively.
*2 Carrier lifetime: decay time of excess electrons and holes to recover the thermal equilibrium. A longer carrier lifetime achieves low-loss current conduction of SiC bipolar devices.
*3 Carbon Interstitial Diffusion Process: a method to eliminate carbon vacancy defects by introduction of carbon interstitials from SiC crystal layer surface followed by thermal diffusion of the interstitials to deep in the layer.
*4 High-Temperature Dislocation Conversion Process: a method to convert BPDs to TEDs by high-temperature annealing in Ar at 1800-2000℃, while BPDs degrade forward current conduction performance of SiC bipolar devices and TEDs are inactive for the degradation.
*5 Direction of disorder of atomic arrangements around a dislocation line.

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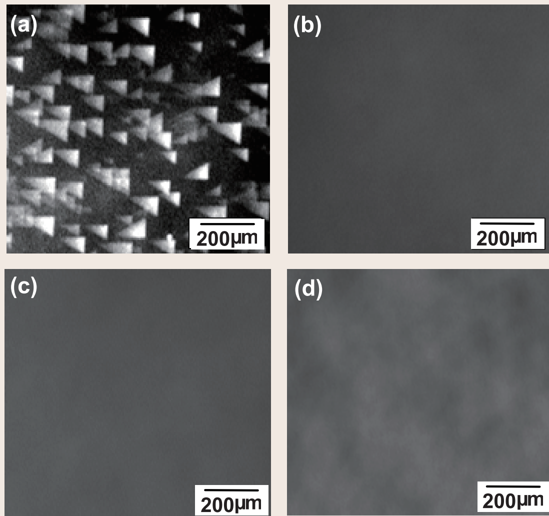

Fig. 1: PL mapping images of SiC crystal layers

PL images of 4H-SiC crystal layers obtained under (a) system pressure of 40 Torr, H_2 flow rate of 40 slm, (b) 40 Torr, H_2 60 slm, (c) 30 Torr, H_2 40 slm, and (d) 200 Torr, H_2 40 slm with the addition of HCl at 3 slm. The PL images were acquired using a 450 nm band pass filter. Triangular defect contrast observed in (a) corresponds to 8H-type stacking faults in the crystal layer, and no 8H-type stacking faults are found in (b), (c) and (d). [slm: standard liter per minute (gas flow rate under the standard temperature and pressure)].

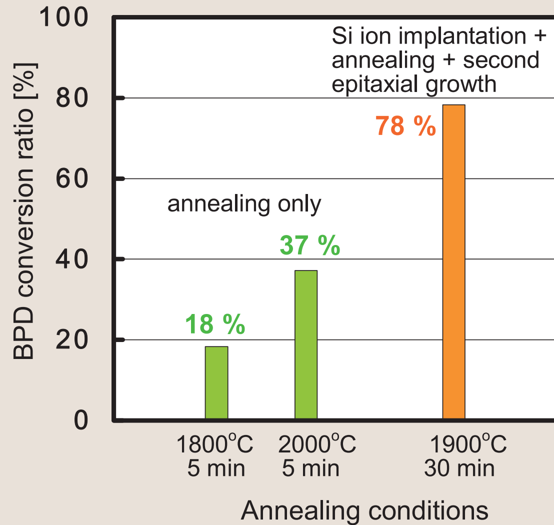

Fig. 2: Conversion ratios of BPDs in “High-Temperature Dislocation Conversion Process”

Conversion ratios of BPDs in “High-Temperature Dislocation Conversion Process” are enhanced by an increase of annealing temperature or performing ion implantation to the layer surface followed by high-temperature annealing and the second epitaxial growth, and a significant reduction of a BPD density in SiC crystal layers is achieved.

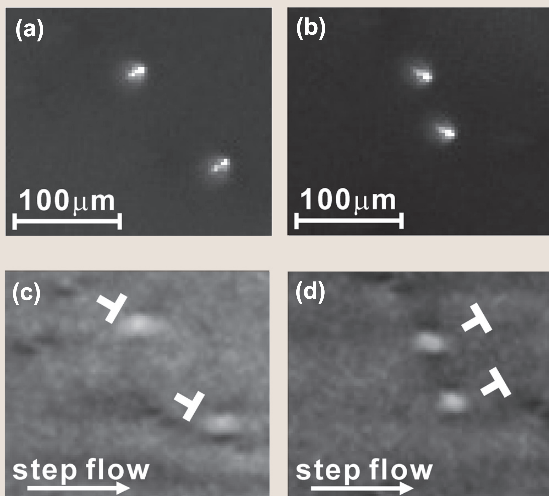

Fig. 3: (a), (b) Plan-view PL images and (c), (d) synchrotron X-ray topography images of TEDs with the two types of Burgers vector

The PL images in (a) and (b) were taken using a 900 nm band pass filter. The “⊤” signs in (c) and (d) indicate the direction of an extra half plane created by a TED, where the direction is identified by the synchrotron X-ray topography images. The PL appearance of the TEDs in (a) and (b) is confirmed to vary according to the direction of an extra half plane, demonstrating the capability of discrimination of the extra half plane of TEDs in 4H-SiC crystal layers by the PL technique.

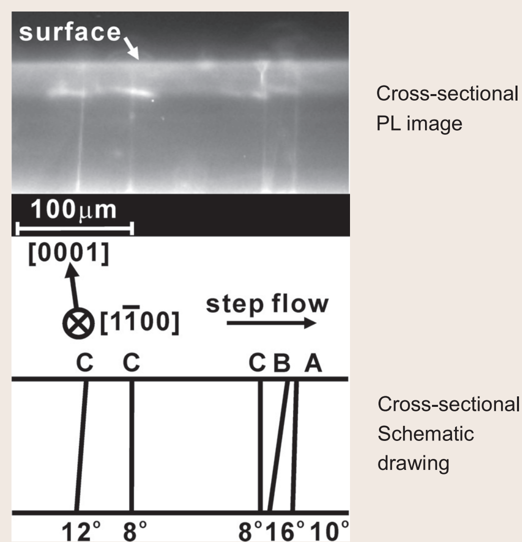

Fig. 4: Cross-sectional PL image of a 4H-SiC crystal layer and schematic drawing of the image

The “A” and “B” lines correspond to TEDs and the “C” line corresponds to a TSD, and the angles indicate the inclination angle from [0001] direction in the schematic drawing. Direct observation of the behavior of TEDs and TSDs propagating toward the surface with an inclination angle in a thick SiC crystal layer is demonstrated.